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Selective Deposition of Ge-rich Si-Ge Layers from Single Source Si-Ge Hydrides

Employing selective epitaxy to grow fully strained Si-Ge alloys in the source and drain (S/D) of a p-type metal-oxide semiconductor (PMOS) transistor compresses the Si-channel to significantly increase the hole mobility, and consequently, the speed of the device. Ge-rich alloys, where Ge constitutes = 50% of the alloy, are of particular interest because of expectations that these alloys will produce disruptive improvements in the saturation/drive currents over traditional, Si-rich, configurations. Still, current selective growth processes are unable to yield films with device quality morphology and microstructure for the desired Ge range. Likewise, conventional processes produce high dislocation densities, non-uniformities in strain, lack of compositional control, and reduced film thickness in Ge-rich films, which ultimately can degrade the quality and performance of the stressor material, subsequently, limiting the practical usefulness of these approaches.

Researchers at Arizona State University have developed a device quality method to selectively deposit Si-Ge materials, specifically Ge-rich Si-Ge materials, on substrates. This method exploits the unexpected and unique growth properties of Si-Ge hydride compounds to selectively deposit Si-Ge layers, for example, as strained-layered heterostructures of Ge-rich semiconductors in the S/D regions of PMOS structures. The method achieves high strain states in Si-Ge layers that are typically much thicker than the nominal equilibrium critical thickness during blanket growth.

Potential Applications

- Semiconductors (e.g. CMOS, NMOS, PMOS, MOSFET, etc.)
  - Microelectronics
- Optoelectronics (e.g. Photodiodes, etc.)

Benefits and Advantages

- Provides Selective Area, Device Quality, Ge-Rich Si-Ge Alloys ? allows selective growth (renders high mobility devices and opens path to III-V integration with Si); produces monocrystalline microstructures, smooth and continuous surface morphologies, and low defect densities; demonstrates 50 ? 75% Ge content compared to the 20 ? 30% content of existing approaches
- Provides High Strain - up to 2.3 % demonstrated in blanket growth and typically much thicker than the nominal equilibrium critical thickness
- Operates at CMOS-Compatible Low Temperatures ? heteroepitaxy at 300 - 450°C
- Offers Simple Integration ? single source precursor eliminates the need for multi-component reactions and corrosive etching processes; high levels of

controllability and uniformity