Skysong Innovations
Advancing the Arizona State University Knowledge Enterprise

1475 N. Scottsdale Road, Suite 200
Scottsdale, AZ 85287-3538
Phone: 480 884 1996 Fax: 480 884 1984

Case ID:M07-097P
Published: 1/25/2011

Inventors

Lawrence Clark

Giby Samson

Contact

Shen Yan
shen.yan@skysonginnovations.com

Dynamic CMOS RAM Decoder with Reduced Access Time, Standby and Active power Dissipation

Random Access Memories (RAM) are read/write memory devices that can read data from or write data to any of its memory addresses. Static random access memories (SRAM) store data in flip-flops, which retain data as long as the SRAM is powered up. SRAMs are one of the VLSI circuit types most amenable to leakage power mitigation techniques. Most of these techniques achieve this objective by focusing on SRAM array leakage. However, up to half of the total SRAM transistor width may be comprised of peripheral circuitry. These peripheral circuits used to perform decode, sense, and write functions are usually constructed based on static NAND and NOR gates. Conventional static CMOS decoders dissipate a significant amount of power, particularly in unselected banks. The decoding step also forms a significant portion of the read access time. Finally, transistor variation is increasing in modern processes, which is manifested as increased timing variation, making conventional, but low access time, SRAM timing more difficult.

Researchers at Arizona State University have developed a fully dynamic decoder with less delay and dynamic power dissipation than conventional designs. The leakage power dissipation is reduced by utilizing the stack effect or dynamically applied PMOS power gating. The decoder also has less clock node capacitive loading and very low capacitive loading to the address lines enabling faster low power address delivery. The address line activity is shielded from the decoder internal nodes by the input stage, thereby providing an activity factor of zero in unselected banks. The power saved by this technique is magnified and forms a significant portion of the total power consumption in large SRAMs with several banks. A prototype chip fabricated implementing this technique has been tested and provided reliable and consistent results that met the above mentioned performance standards.

Potential Applications

- SRAM and DRAM fabrication
- Flash memory storage devices
- Solid state memory devices such as mp3 players

Benefits and Advantages

- Significant improvement in power dissipation ? up to 5 times less than state of the art techniques
- Offers 50% better energy delay
- Reliable performance in deep submicron processes
- Provides an activity factor of zero in unselected banks
- Improves access time and critical race free sense timing

- Allows faster lower power address delivery