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A Robust Asynchronous Scan Chain and Scanning Mechanism for Testing of Digital VLSI Circuits

Very-large-scale-integration (VLSI) is a process of creating massive integrated circuits which enables design of all integrated circuit (IC) components onto a single chip. Thousands of transistors are combined onto a single chip, necessitating highly efficient data scanning in and out of each circuit. Typically the scan-in and scan-out operations are performed at the same time. Data bits stored in each transistor are pulled from the output as new data is introduced to into the chain through the input. Thus, data must be held within the transistor for a certain amount of time (the hold time). When the hold time is violated, the IC will fail. Specialized buffers and increased surface area to accommodate data routing area are therefore needed to ensure the hold time is not violated.

Researchers at Arizona State University have invented a new scanning mechanism for testing digital circuits. Scanning the data serially in and out of the chip is indispensable for functional testing of ICs post manufacture. The main advantage of this proposed scanning mechanism is the elimination of hold time violation in the side-chain during test/scan mode. The scanning mechanism operates asynchronously, so the synthesis and automatic layout tools do not have to optimize timing related to the scanning mechanism. Buffers and routing area on the integrated circuit are also minimized through elimination of the single global test-enable signal.

Potential Applications

- Data scanning
- VLSI circuits
- Process controls
- Computing
- Circuit design
- Semiconductors
- Electronics

Benefits and Advantages

- Speed – Circuit Hold time violation in the scan-chain during test/scan mode is eliminated.
- Low Cost –
  - Easily integrated into existing manufacturing processes.
  - Elimination of separate scan clock device, lowering manufacturing costs.
  - Functional testing of circuits post-manufacture.
- Smaller Size – Elimination of a single global test-enable signal reduces the necessary routing resources (i.e. buffers and routing area)

For more information about the inventor(s) and their research, please see

Dr. Sarma Vrudhula's directory webpage

For more information about related technologies, please see

M15-192P: A Robust Edge-Triggered Thershold Logic Flipflop (PNAND) with Scan, Preset, and Clear

M15-193P: An Energy Efficient, Robust Differential Mode D-FLip-Flop (KVFF)