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Non-Volatile Logic Device for Energy-Efficient Logic State Restoration

Background

Microelectronic circuits that obtain their energy from ambient energy sources (AES) through scavenging or harvesting are increasing in popularity, particularly with the burgeoning field of the Internet of Things (IoT). Some of the more common AES include solar, piezoelectric, vibration, airflow, and thermoelectric.

The intermittent nature of the energy delivered by AES poses a challenge for microelectronic systems as they are generally architected for continuous operation. Conventional digital technology, including logic and memory (SRAM or DRAM), is volatile, such that information (e.g., a state of the computation and a state of memory) is lost when the power supply is disrupted. Due to the intermittent nature of AES, accurately predicting an impending power disruption and saving a current state is desired for most devices.

In non-volatile memory (NVM), the stored information is retained even when there is no power. With conventional NVM technology, the state of logic and memory has to be saved in an off-chip storage and restored when power is re-established. For example, a processing unit (e.g., a microcontroller) can be enhanced with an NVM array (NVMA), which is separate from the local (volatile) registers where the intermediate computation results of the processing unit are stored. Before the power failure, the data in all the registers is saved serially in the NVMA and later serially restored. This technique incurs high energy cost and a long backup time, and is typically not suitable for a system powered by AES.

Invention Description

Researchers at Arizona State University have developed a non-volatile logic device for energy-efficient logic state restoration. In place of an off-chip non-volatile memory array (NVMA), each register in a processing unit (e.g., a microcontroller) can be a non-volatile flip-flop (NVFF), which operates similar to a regular flip-flop in a normal mode, but has the added capability of storing its state in a local non-volatile device before a power failure. This innovation describes a circuit architecture for a NVFF which incorporates a volatile flip-flop and a non-volatile storage unit to achieve on-chip non-volatile storage. The non-volatile logic device further allows for the backup time to be determined on a per-chip basis, resulting

in minimizing energy wastage and satisfying a given yield constraint.

In an exemplary aspect, the non-volatile logic device employs spin-transfer torque magnetic tunnel junctions (STT-MTJ) as a non-volatile device. A STT-MTJ device may operate with a critical current being delivered for some minimum duration in order to switch a state of the STT-MTJ. Other examples may use other compatible non-volatile logic devices, such as spin orbit torque magnetic tunnel junctions (SOT-MTJ).

An exemplary embodiment relates to a non-volatile logic device on a semiconductor die. The non-volatile logic device includes a volatile scan flip-flop and a non-volatile storage unit coupled to the volatile scan flip-flop. During a backup mode, the non-volatile storage unit stores a state of the volatile scan flip-flop. Upon loss of power to the non-volatile logic device, the non-volatile storage unit retains the stored state.

Another exemplary embodiment relates to a non-volatile flip-flop. The non-volatile flip-flop includes a volatile flip-flop and a non-volatile storage unit coupled to the volatile flip-flop. The non-volatile storage unit includes a data STT-MTJ configured to store a state of the volatile flip-flop during a backup mode and be inactive during a normal mode.

This innovation is covered by U.S. Pat. No. 10,795,809.

Potential Applications

- Non-volatile memory
- Resistive random-access memory (RRAM)
- Internet-of-Things (IoT)

Benefits and Advantages

- Design allows for backup time to be determined on a per-chip basis
- Near-instant backup and restoration
- Minimizes energy usage
- Allows a computation to be interrupted midstream and resumed where it was suspended, with minimal hardware overhead for the control unit