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Dividerless Phase-Locked Loop with Sampled Lowpass Filtering

Background

The growing market for wearable, portable, and implantable devices has understandably led to increasing demand for low-power, compact electronics. High-speed data transmission requires phase-locked loops (PLLs) capable of carrier frequency generation with extremely low noise. The challenge of balancing oscillator noise performance with area has motivated the development of sub-sampling phased-locked loops (SSPLLs). SSPLLs do not require explicit frequency divider circuitry in the core loop, and thus do not exhibit the phase detector (PD)/charge pump (CP) N2 noise that dominates the in-band noise of traditional PLLs. However, SSPLLs rely on highly accurate, high-speed analog sampling of the voltage-controlled oscillator (VCO) output waveform. This places significant constraints on the design of the sampling circuitry, often translating to large power and area overheads. Additionally, because many SSPLL architectures require the CP to be able to provide an analog range of currents, a CP that is not entirely linear will cause nonlinearity in the overall loop dynamics.

Invention Description

Research at Arizona State University has led to the development of a novel phase-locked loop architecture that is capable of wideband, dividerless, reconfigurable integer-N synthesis. This architecture retains the same loop transfer function as an SSPLL while also removing the PD/CP N2 noise that dominates the in-band noise of traditional PLLs. The resulting noise reduction allows the presented PLL to operate with integrated jitter as low as 250fs. Unlike SSPLLs however, the sampling block is placed downstream of the PD/CP, reducing the effects of aperture and pedestal error by the gain of the CP/PD. This architecture requires only low-frequency sampling blocks, effectively removing the power and area overheads associated with direct sampling of the VCO.

Diagram of one embodiment of the dividerless PLL

Potential Applications

- Phase-locked loops

- Frequency synthesis blocks
- Electronic systems requiring accurate timing
- Wearable and Internet-of-Things (IoT) electronics

Benefits and Advantages

- Avoids area and power overheads associated with sub-sampling of the VCO
- Increases device efficiency and battery life
- Achieves best-in-class figure of merit (FoM) among state-of-the-art technologies with similar oscillator topologies