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Pulse-Clocked TMR Flip-Flop Design for Efficient Temporal Radiation Hardening of Digital Circuits

Digital circuits use sequences of logic gates called flip-flops (FFs) to store and transmit binary information. Triple mode redundant (TMR) FFs have three logic gates that produce a single output based on their majority state in case one fails due to soft error. A soft error occurs when a switch within a digital circuit flips to its opposite state, thereby transmitting an incorrect signal. Particles energized by radiation can cross several circuit nodes and trigger multiple simultaneous soft-errors, so TMR FF nodes must be spaced far enough apart to prevent concurrent malfunctions. On the other hand, pulse-clocked FFs are much smaller and more energy efficient than standard FFs, but they must operate synchronously under a global clock (CLK) signal. So when a soft error occurs in the CLK, it propagates through all the FFs controlled by the CLK. To harden against CLK soft errors, signal delay filters can be installed such that the FFs offset the timing (temporal) difference within a sample of clock pulses. However, delay filters consume additional energy and physical space, making current designs considerably inefficient and bulky

Researchers at ASU have designed temporally hardened, pulse-clocked TMR FF circuitry that reduces semiconductor size and energy consumption. The circuitry configuration consists of a temporal pulse generator that drives multiple TMR FFs. Not only does this configuration minimize layout area, it results in faster processing speeds due to lower clocking overhead. TMR FF components are interleaved throughout the circuitry, which enforces the node separation needed to prevent multiple node charge collection (MNCC) from simultaneous soft-errors without taking up any additional space. The pulse generator implements fewer delay filters than in current designs, further decreasing circuit size and energy consumption. The pulse-clocked TMR FFs are also compatible with integrated clock gating schemes for added power savings.

Potential Applications

- Electronic Components for
  - Spacecraft
  - Satellites
  - Nuclear Reactors
- Integrated Circuit CAD Software
- Radiation Hardened Digital Circuits

Benefits and Advantages

- Efficient – Faster processing speeds due to lower clocking overhead.
- Inexpensive – Smaller integrated circuits reduce semiconductor material

costs.

- Innovative – Pulse generator implements fewer delay filters than current designs
- Practical
  - Compatible with integrated clock gating schemes.
  - Interleaving TMR FF components enforces node spacing for MNCC prevention without taking up any additional physical space.
- Smaller
  - Fewer delay filters decrease size of pulse generator.
  - Multiple TMR FFs per pulse generator minimizes layout area.

For more information about the inventor(s) and their research, please see

Dr. Lawrence Clark's directory webpage