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Hysteresis Control Loop for Three-Level Switching Converters

Background

Three-level converters are used in various power management applications such as DC-DC converters, average power tracking (APT), and envelope tracking modulators to efficiently regulate output voltage to a voltage different from the supply voltage. Advantages of three-level converters include low output current ripple, smaller off-chip inductor, and higher supply voltage tolerance than two-level converters. Conventionally, a pulse-width modulation (PWM) approach is used to control the loop and power devices in three-level converters by using two 180-degree phase-shifted synchronization signals. However, PWM control loops have a number of disadvantages that make three-level converters less appealing, including (1) susceptibility to instability that requires compensation circuits, (2) low loop bandwidth that is a fraction of switching frequency, (3) requirement of an additional calibration loop to regulate the voltage across the flying capacitor which is a part of the three-level converter, and (4) requirement of on-chip or off-chip synchronization of PWM signal generators which need to be precisely controlled and phase shifted.

Invention Description

Researchers at Arizona State University have developed a hysteresis-controlled three-level switching converter in parallel with a class-AB, slew-rate-enhanced linear amplifier (LA) to produce an 80MHz BW, 91%-efficient, hybrid envelope-tracking modulator (ETM). Specifically, four key advantages characterize this converter:

(1) The hysteresis loop is inherently stable across a wide load range and does not require compensation circuit. Thus, by simplifying loop design, a higher-speed loop and a wider-bandwidth converter can be achieved.

(2) The loop bandwidth in hysteresis control is as high as switching frequency; therefore, the converter does not contribute to higher switching losses.

(3) No synchronization signal is required, whereas in PWM control loops, timing accuracy of the synchronization signals is a limiting factor in increasing the switching frequency.

(4) The flying capacitor voltage VCF is sensed and regulated in the main control

loop on every cycle. Therefore, the requirement for an extra calibration loop is eliminated in this proposed technique, and the controller ensures VDD/2 voltage across the switches to prevent over-stressing of thin-gate transistors.

The LA uses slew-rate enhancement (SRE) to achieve a slew rate above 325V/μs and BW up to 275MHz, allowing ETM operation at LTE-80MHz.

Potential Applications

- DC-DC converters
- Average power tracking
- Envelope tracking

Benefits and Advantages

- Innovative – First use of hysteresis control loop for three-level converters
- High Performance – Hysteresis-controlled loop bandwidth is 2-3 times that of PWM-controlled loop, and can be as high as switching frequency
- Compact – Reduction of off-chip components results in small size and possibility of full integration

Related Publication 1

Related Publication 2