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Clock Skewing for Area and Power Optimization of ASICs Using Differential Flipflops and Local Clocking

Synchronous logic remains the dominant design paradigm of digital systems such as Application Specific Integrated Circuits (ASICs). The conventional design of sequential circuit networks is based on the assumption that every register receives the clock signal at the same time. However, guaranteeing the simultaneity of clock arrival times in practice is not possible due to the presence of the gate and interconnect delays, resulting in clock skew. Many techniques have been developed to combat this issue, such as 1) designing the clock distribution network to achieve zero skew, 2) modifying gate sizing to meet the timing requirements, or 3) deliberately manipulating skews to improve performance. Deliberate clock skewing by adding buffers, however, remains difficult due to the precision of required delays and the possibility of hold time violations. Additionally, these existing solutions are expensive due to the extra power consumption of buffers and load on the clock tree, presenting another challenge for optimizing system performance while minimizing costs.

Researchers at Arizona State University have developed a design methodology for reducing area and power (both static and dynamic) of standard ASICs that uses a combination of differential flipflops and a deliberate clock-skewing, referred to as Local Clocking (LC). LC is based on deliberately introducing clock skew without the use of extra buffers in the clock network. This is achieved through the use of some flipflops, called sources, generating clock signals for other flipflops, called targets. This method includes two key features: (1) a uniquely designed differential flipflop (referred to as KVFF and functionally identical to a master-slave edge-triggered D flipflop) that produces a completion signal that is a skewed version of its input clock, which is used to clock other flipflops; and (2) an efficient algorithm that identifies the sources and targets involved in the new clocking scheme, with the objective of reducing area and power.

Deliberate skew introduced by LC creates extra slack on logic cones, reducing area and power through synthesis tools and eliminating the need for conventional methods like buffers. Preliminary testing showcases consistent improvements in area, power, and wirelength, and LC has proved effective in eliminating hold-time violations, thus marking a significant advancement in optimizing digital system performance.

Related publication: A New Approach to Clock Skewing for Area and Power Optimization of ASICs Using Differential Flipflops and Local Clocking

Potential Applications:

- ASIC circuit manufacturing
- Semiconductor manufacturing

Benefits and Advantages:

- Significant improvement in area and power of digital systems
- Low-cost solution to clock skew
- Eliminates hold-time violations
- Maintain performance of ASIC circuits while minimizing clock skew
- Can be used as an additive to existing power reduction techniques such as clock and power gating