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Fast Parallel Test of SRAM Arrays

Static random access memory (SRAM) is used extensively in modern integrated circuits, comprising over 90% of the transistor count in server microprocessors. Over the past couple decades, technology has aggressively scaled down integrated circuit components, quickly entering the nanoscale. At this scale of manufacturing, there is inevitably an increase in fabrication variation leading to increased failure rates. In order to ensure a level of quality performance, testing must be performed on the chips. This is time intensive and expensive, ultimately costing as much as 1/3 of the total production costs.

Researchers at Arizona State University have developed a method of parallel testing that could greatly decrease the time and therefore cost of testing SRAM. The technology works by pre-conditioning the cells to one state in parallel, and then applying parallel stress to the cells, in this way stability parameters such as read margins, write margins, and other cell stability parameters can be determined on a massively parallel basis, feasibly increasing the test speed by more than 1,000 times over conventional methods.

Potential Applications

This technology applies to any company that manufactures SRAM which is used in products such as:

- Personal Computers
- Routers
- Digital Cameras
- Cell Phones
- Other Handheld Electronic Devices

Benefits and Advantages

- Drastically decrease test time in turn increasing production
- Decrease testing costs by up to 50%
- Potentially over 1,000 times faster than conventional testing methods