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FPGAs with Reconfigurable Threshold Logic Gates for Improved Performance, Power, and Area

Invention Description

Implementation of lookup tables (LUTs) in a field-programmable gate array (FPGA) comes at the heavy cost of area, power, and performance. Researchers at Arizona State University have developed an alternative FPGA tile structure that consists of three traditional LUTs combined with a new reconfigurable threshold logic cell (TLC). The TLC requires only 7 static random-access memory (SRAM) cells and can be configured to implement one of several threshold functions. Results demonstrate an average reduction of 8.9% in register count, 15.4% in multiplexer count, 7% average reduction in Basic Logic Element (BLE) area, and 8.2% average reduction in BLE power. Without loss in performance, maximum reductions in the following parameters have been achieved: Register count, 64%; BLE multiplexer count, 68%; BLE area, 51.6%; BLE power, 61.6%; and tile area, 21%. The architecture is implemented in a 28nm Fully Depleted Silicon on Insulator (FDSOI) process, and is evaluated on standard benchmark circuits and several large complex function blocks.

Potential Applications

- Field-programmable gate arrays (FPGAs)

Benefits and Advantages

- Provides simultaneous improvements in area, power, and performance for LUT-based FPGA architectures

Related Publication

Faculty Profile of Professor Sarma Vrudhula