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Low complexity Out-of-Order Issue Logic using Static circuits

Instruction-level parallelism (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously. Superscalar techniques based on extracting instruction-level parallelism have been a major contribution to high performance microprocessor design throughout the last decade. The number of instructions executed per cycle (IPC) is increased substantially through superscalar techniques like speculative execution and dynamic scheduling. While speculative execution deals with control dependencies, dynamic scheduling processes data dependencies and leverages the stalls due to dependencies through out-of-order execution. The out-of-order issue logic identifies if instruction operands are ready and selects the highest priority ready instructions for execution. Despite these advantages however, there is still demand for more efficient and less complex methods to resolve issue logic complexity.

Researchers at Arizona State University have developed a new method to reduce issue logic complexity. They have developed a novel issue logic implementation that divides the instruction ready signals into groups and selects the four highest priority instructions. By splitting the ready signals into groups and processing them in parallel, the complexity of issuing multiple instructions is reduced. The oldest first priority selection is used and the wakeup, update and select operations are completed in a single cycle ensuring high instructions per cycle (IPC). The select and update logic are implemented using static combinational logic that aids in borrowing time from wakeup logic. The design is implemented entirely in static CMOS circuits to reduce the power dissipation and provide ease of implementation as well as process portability. The method also reduces low fan out and improves circuit speed.

Potential Applications

Microprocessor manufacturers such as:

- Advanced Micro Devices (AMD)
- Intel
- ARM
- IBM
- Broadcom Corporation

Benefits and Advantages

- Less power consumption
- Faster circuit speed
- Simple architecture
- Ease of implementation
- Process portability